SPECIFICATION

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[CONTROL CHIP AND METHOD FOR ACCELERATING MEMORY ACCESS]

Cross Reference to Related Applications

This application claims the priority benefit of Taiwan application serial no. 91103729, filed on March 1, 2002.

Background of Invention

[0001] Field of Invention

[0002] The present invention relates to a control chip. More particularly, the present invention relates to a control chip and method for accelerating memory access.

[0003] Description of Related Art

[0004]

Following the rapid progress in electronic technologies, people rely heavily on the processing capability of various electronic devices. In general, electronic devices operate in a distributed environment. In a distributed environment, a control chip communicates data with a central processing unit (CPU) through a system bus. The amount of information transferred between the two increases as the processing power of the CPU increases. Correspondingly, the number of data bits and address bits that needs to be transferred via the system bus also increases. To prevent a corresponding increase in the pin count of a CPU, the data bits and address bits are transmitted in a number of bus clock cycles. However, for this type of data transfer, the memory read command received by the control chip must be received after the memory write command in the memory write command queue having the same write-in address is transferred, otherwise, memory read errors may occur. Thus, the control chip must

wait until all the separately transferred bit addresses have arrived and been compared with the write address of the memory write command stored inside the memory write command queue before execution. Consequently, processing speed of the control chip is severely lowered. In addition, the control chip uses a rather complicated method to process the memory read commands. Hence, performance of the control chip is relatively low.

Summary of Invention

[0005] Accordingly, one object of the present invention is to provide a control chip and an operating method for accelerating memory access. By increasing the processing speed of memory read commands, performance of the control chip is increased. Furthermore, the memory read command received by the control chip is also prevented from executing before the memory write command stored inside the memory write command queue with an identical write address is executed.

[0006]

To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a control chip for accelerating memory access. The control chip is coupled to at least one system bus operating with a clock signal. The control chip includes a memory write command queue, a bus interface unit and a memory request organizer. The memory-write command queue is used to hold a plurality of memory write commands. Each memory-write command further includes a write address. The bus interface unit is coupled to the system bus. The system bus sequentially receives the first section read address and the second section read address according to the clock signal and then outputs the first section read address and the second section read address. The memory request organizer is coupled to the bus interface unit and the memory-write command queue for comparing the first section read address with an identical bit portion of the write address of the memory write commands inside the memory write command queue. If the result of comparison shows that they are different, execution of the memory read command is granted. On the other hand, if the result of comparison shows that the are identical, a second comparison is carried out to compare the second section read address with an identical bit portion of the write address of the write commands inside the memory-write command queue. If the

result of second comparison shows that they are different, execution of the memory read command is granted. On the other hand, if the result of second comparison shows that they are identical, execution of the memory read command is granted only after the memory-write command inside the memory-write command queue having an identical write address is executed.

[0007] This invention also provides a control chip having a memory request organizer for accelerating memory access. The memory request organizer includes a first section address read/compare unit, a second section address read/compare unit and a grant decision unit. The first section address read/compare unit is coupled to a bus interface unit and a memory-write command queue. The first section address read/compare unit receives a first section read address, compares the first section read address with an identical bit portion of the memory address of the memory-write command inside the memory-write command queue and outputs a first comparison signal. The second section address read/compare unit is coupled to the bus interface unit and the memory-write command queue. The second section address read/compare unit receives a second section read address, compares the second section read address with an identical bit portion of the memory address of the memory-write command inside the memory-write command queue and outputs a second comparison signal. The grant decision unit is coupled to the first section address read/compare unit and the second section address read/compare unit. The grant decision unit receives the first comparison signal and the second comparison signal to generate a grant signal. If the first comparison signal or the second comparison signal indicates a difference in the comparison, the grant decision unit issues a grant signal. Otherwise, the grant decision unit issues a grant signal only after the memory-write command inside the memory-write command queue having an identical write address is executed.

[0008] This invention also provides a control chip having a memory request organizer for accelerating memory access. The memory request organizer further includes a memory command control unit coupled to the grant decision unit for receiving a grant signal and directly transmitting a memory read command into or out of a memory read command queue.

[0009] In one embodiment of this invention, the system bus is a S2K bus as defined by the corporation AMD. Furthermore, the system bus is connected to a K7 series central processing unit of AMD. Each rising edge and falling edge of the clock signal in the system bus is defined to be a single bit time unit and the first section read address is transmitted in two bit time units.

[0010] This invention also provides a method of operating a control chip connected to a system bus such that memory access is accelerated. The control chip at least includes a memory-write command queue for holding a plurality of memory-write commands. Each memory-write command includes a write address. The system bus at least includes a clock signal capable of sequentially transmitting the first section read address and the second section read address of a memory read command. The method of operating the control chip includes the following steps. First, the control chip picks up a first section read address from the system bus. The first section read address is compared with the identical bit portion of the write address of the memory-write command inside the memory-write command queue. If the comparison indicates a difference, execution of the memory read command is granted. The control chip then picks up the second section read address from the system bus. The second section read address is compared with the identical bit portion of the write address of the memory-write command inside the memory-write command queue. If the comparison indicates a difference, execution of the memory read command is granted. On the other hand, if the comparison indicates the two are actually identical, execution of the memory read command is granted only after the memory-write command inside the memory-write command queue having an identical write address is executed.

[0011] In the operating method according to this invention, the rising edge and the falling edge of a clocking cycle in the system bus are each defined to be a single bit time unit. The first section read address is transmitted in two bit time units. When execution of the memory read command is granted, the memory read command is directly transmitted into or out of a memory read command queue.

[0012] The application of the control chip and operating method according to this invention is able to speed up memory access. As soon as the control chip receives the

first section read address, the first section read address is immediately compared with an identical bit portion of the write-in commands inside the memory-write command queue. The execution of memory read command is immediately granted if the comparison indicates a difference. If the comparison indicates identical bits, the control chip picks up the second section read address and compares the second section read address of the memory read command with an identical bit portion of the write-in commands inside the memory-write command queue. The execution of memory read command is also granted if the comparison indicates a difference. On the other hand, if the comparison still indicates the presence of identical bits, execution of the memory read command is delayed until the memory-write command inside the memory-write command queue having an identical write address is executed. In this way, execution of each memory read command need not wait until all bit addresses necessary for separate transmissions have arrived. Hence, performance of the control chip is improved and execution of a memory read command received by the control chip before the execution of a memory-write command inside the memory-write command queue having an identical write address is prevented.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0015] Fig. 1 is a block diagram showing the components and interconnections inside a control chip capable of accelerating memory access according to one preferred embodiment of this invention;

[0016] Fig. 2 is a listing showing the definition of separate address transmission of a S2K bus according to the preferred embodiment of this invention;

[0017] Fig. 3 is a timing diagram showing various signal traces produced by the control chip according to the preferred embodiment of this invention; and

Sub A1 [0018] Fig. 4 is a flow chart showing the steps for operating the control chip according to the preferred embodiment of this invention.

Detailed Description

[0019] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0020] Fig. 1 is a block diagram showing the components and interconnections inside a control chip 100 capable of accelerating memory access according to one preferred embodiment of this invention. The control chip 100 not only enhances memory access performance, but also prevents the execution of any memory read command before executing the memory-write command inside the memory-write command queue having an identical write address. As shown in Fig. 1, the control chip 100 includes a memory-write command queue 190, a bus interface unit 130 and a memory request organizer 140. The memory request organizer 140 further includes a first section address read/compare unit 150, a second section address read/compare unit 160 and a grant decision unit 170. A memory command control unit 180 may also be incorporated to interface with the grant decision unit 170. The memory-write command queue 190 is capable of holding a plurality of memory-write commands. Each memory-write command has a write address. The bus interface unit 130 is coupled to a system bus 120. The system bus 120 is a S2K bus connected to a K7 series central processing unit 110 manufactured by AMD, for example. The S2K bus has a system address output clock signal line SADDOUTCLK and a system address output bus SADDOUT. The central processing unit 110 transmits the actual address from SADDOUT[14:2] in separate transmissions according to the rising edge and the falling edge of the system address output-clock signal. The rising edge and the falling edge of the system address output clock signal is defined to a single bit time. The transmission format is shown in Fig. 2. As shown in Fig. 2, each memory read command requires four bit times. In bit time zero, bits 31 ~ 25 (PA[31:25]) of the

actual address are transmitted. In bit time one, bits 24 ~ 12 (PA[24:12]) of the actual address are transmitted. In bit time three, bits 34 ~ 32 and bit 11 ~3 (PA[34:32] and PA[11:3]) of the actual address are transmitted. Hence, when the bus interface unit 130 receives the memory read command from the system bus 120, the actual address of the memory read command is also obtained from SADDOUT.

[0021] To provide a deeper explanation of control chip operation, refer to the timing diagram in Fig. 3. In fact, Fig. 3 is a timing diagram showing various signal traces produced by the control chip according to the preferred embodiment of this invention. When SADDOUT transmits the actual address PA[31:25] in bit time zero, AIB01 of the bus interface unit 130 is refreshed. When SADDOUT transmits the actual address PA [24:12] in bit time one, AIB02 of the bus interface unit 130 is refreshed. Similarly, the content transmitted during bit time two will refresh AIB03 of the bus interface unit 130 and the actual address PA[34:32] and PA[11:3] transmitted during bit time three will refresh AIB04 of the bus interface unit 130. Note that frequency of AIBT01 of the bus interface unit 130 is half of SADDOUTCLK. Hence, after the bus interface unit 130 receives the actual address PA[31:12] at bit time zero and bit time one, the first section read address[31:12] of the memory read command is refreshed through Cqfc_ReqAddr. As shown in label 310 of Cqfc_ReqAddr in Fig. 3, the bus interface unit 130 coupled first section address read/compare unit 150 picks up the first section read address[31:12]. Thereafter, the first section read address[31:12] is compared with identical bit portion of write address of the memory-write commands inside the memory-write command queue to output a first comparison signal HHIT to the grant decision unit 170. If the first comparison signal HHIT indicates a mismatch between identical bits, the grant decision unit 170 submits a grant execution signal MRQDREQ in bit time zero of the next command as shown in label 320. On receiving the grant execution signal MRQDREQ, the memory command control unit 180 transfers the memory read command into a memory read command queue 195. Alternatively, the signal DADS is enabled so that the actual address of the memory read command is placed on the KA bus and transmitted to a memory controller. In the meantime, the memory controller responds with a DNA signal.

[0022] On the other hand, if the first comparison signal HHIT indicates the first section read address[31:12] is identical to the bit portion of the write address of the memory-

write commands inside the memory-write command queue after the comparison, actual address PA[11:3] received by the bus interface unit 130 during bit time three is compared. The actual address PA[11:3] will refresh the second section read address PA[11:3] of the memory read command through Cqfc_ReqAddr and enable Cqfc_ReqValid signal to signify the end of address transmission as shown in label 330 of Fig. 3. The second section read address PA[11:3] is picked up by the second portion address read/compare unit 160 coupled with the bus interface unit 130. Bits PA[11:6] inside the second portion read address is compared with identical bits of the write address of the memory-write commands inside the memory-write command queue to produce a second comparison signal LHIT. The second comparison signal LHIT is transferred to the grant decision unit 170 coupled next to the second portion address read/compare unit 160. Note that only bits PA[11:6] are compared in this embodiment because the central processing unit generally accesses the memory in batches. If the second comparison signal LHIT indicates some bit difference, the grant decision unit 170 enables the grant execution signal MRQDREQ. However, if the second comparison signal LHIT indicates the bits are still identical, the grant execution signal MRQDREQ is output only after the memory-write command inside the memory-write command queue having an identical write address is executed.

[0023] According to the aforementioned description, a method of operating the control chip to accelerate memory access is gathered. The method is capable of improving the performance of the control chip and preventing the execution of a memory read command received by the control chip before the memory-write command inside the memory-write command queue having an identical actual address is executed. Actual address of the memory read command comes from the system but S2K. The system bus S2K has a system address output clock signal line SADDOUTCLK. According to the rising edge and the falling edge of the system address output clock, the actual address is transferred from the system address output bus SADDOUT of the system bus S2K in separate synchronized transmissions. The rising edge and the falling edge of the system address output clock signal is defined as bit time.

[0024] Fig. 4 is a flow chart showing the steps for operating the control chip according to the preferred embodiment of this invention. First, the control chip receives a first section read address PA[31:12] (S405) from the system address output bus SADDOUT.

The first section read address PA[31:12] is compared with identical bit portion of the write address of the memory-write command inside the memory-write command queue (S410). If the comparison indicates some difference, execution of the memory read command is granted (S430). If the comparison indicates the bits are identical, the second section read address PA[11:3] on the system address output bus is received (S415). The second section read address PA[11:6] of the memory read command is compared with an identical bit portion of the write address of the memory-write commands inside the memory-write command queue (S420). If the comparison indicates some difference, execution of the memory read command is granted (S430). However, if the comparison indicates the presence of identical bits, execution of the memory read command is granted (S430) only after the memory write command inside the memory-write command queue having an identical write address is executed (S425). Note that as soon as the first comparison signal HHIT indicates a difference, the signal MRQDREQ signal is enabled during bit time zero in the next read command so that execution of the read command is granted instead of having to wait for the result of the second comparison LHIT. Hence, the command is read one clocking cycle ahead, thereby improving the performance of the control chip.

[0025] In one embodiment of the method of operating a control chip to accelerate memory access, the first section read address is transmitted during bit time zero and bit time one. After granting the execution of the memory read command, the memory read command is directly output or transferred to the memory read command queue 195 for storage.

[0026] In conclusion, the control chip and operating method for accelerating memory access includes performing an immediate comparison between a portion of the bit address PA[31:12] with an identical bit portion of the write address of the memory-write commands inside the memory-write command queue as soon as the control chip receives the bit address PA[31:12] during bit time zero and bit time one. If the comparison indicates some difference, permission to execute the memory read command is granted. Execution of each memory read command need not wait for the arrival of all bit address transmitted in separate transmissions. Ultimately, the memory read command may execute one cycle ahead so that performance of the control chip is greatly boosted.

[0027] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.